Abraham Farrell

afarrell538@gmail.com
github.com/abe-f
linkedin.com/in/abrahamfarrell

Education

M.S. in Computer Science | **University of Illinois Urbana-Champaign** 2023–2026
Advisor: Josep Torrellas | Research Area: Computer Architecture Urbana, IL

B.S. in Computer Engineering | **Binghamton University** 2019–2023
In-Major GPA: 3.99 Binghamton, NY

Industry Experience

CPU Microarchitecture Exploration Intern Summer 2025
Arm Raleigh, NC

- Investigated TSO consistency for x86 emulation in a future-generation CPU core.
- Correlated C++ load-store unit performance model with RTL and implemented new features.
- Implemented write coalescing buffer improvement for >15% IPC improvement in TSO mode.
- Conducted several studies on filter caching for L1D$ bank conflict reduction.

CPU Microarchitecture Exploration Intern Summer 2024
Arm Austin, TX

- Characterized and mitigated microarchitectural performance instability.
- Created tool to automatically identify sources of noise using performance counters.
- Identified unstable predictor in the L2$ subsystem responsible for >20% of performance instability.
- Improved performance and stability of the unstable predictor using C++ performance model.

CPU Performance Intern Summer 2023
Arm Austin, TX

- Investigated automatic performance analysis techniques for Arm's high-performance cores.
- Created a hierarchical decision tree-based bottleneck analysis tool using Python.

Hardware Applications Engineering Intern Summer 2022
Arm Austin, TX

Academic Experience

Graduate Research Assistant August 2023 – June 2026
University of Illinois Urbana-Champaign Urbana, IL

- Advisor: Josep Torrellas
- Research in scalable hardware and software for manycore CPUs.
- Collaborated with Intel to investigate NUMA-related performance bottlenecks in database systems.
- Characterized memory system bottlenecks in MySQL on a multi-socket Sapphire Rapids CPU using hardware performance counters.
- Contributed to scalable coherence for chiplet-based CPUs (ISCA '26), on-chip accelerator chaining for datacenter workloads (HPCA '26), and programmable processing-using-memory (HPCA '26).

Undergraduate Researcher September 2021 – May 2023
Binghamton University Binghamton, NY

- Advisor: Dmitry Ponomarev
- Research in computer architecture and security.
- Implemented a cache partitioning technique in Verilog (paper appeared in NDSS '24).

Undergraduate Course Assistant August 2021 – December 2021
EECE 351 – Digital Systems Design Binghamton, NY

- Topics: FPGA design, timing analysis, FSMs, FIFOs, memory, verification

Publications

[1] Jovan Stojkovic, **Abraham Farrell**, Gerasimos Gerogiannis, Zhangxiaowen Gong, Christopher Hughes, and Josep Torrellas. **Dorado: Clustered Hardware Cache Coherence for 1,000+ Cores**. In *Proceedings of the 53rd International Symposium on Computer Architecture (ISCA)*, 2026.

[2] Charles Block, Pedro Palacios, **Abraham Farrell**, Gerasimos Gerogiannis, and Josep Torrellas. **Performance-Driven Composite Prefetching with Bandits**. *4th Data Prefetching Championship (DPC4)*, 2026.

[3] Jovan Stojkovic, **Abraham Farrell**, Zhangxiaowen Gong, Christopher J. Hughes, and Josep Torrellas. **AccelFlow: Orchestrating an On-Package Ensemble of Fine-Grained Accelerators for Microservices**. In *Proceedings of the 32nd International Symposium on High-Performance Computer Architecture (HPCA)*, 2026.

[4] Minh S. Q. Truong, Yiqiu Sun, Dawei Xiong, Amol Shah, Alexander Glass, **Abraham Farrell**, James A. Bain, L. Richard Carley, and Saugata Ghose. **The Memory Processing Unit: A Generalized Interface for End-to-End In-Memory Execution**. In *Proceedings of the 32nd International Symposium on High-Performance Computer Architecture (HPCA)*, 2026.

[5] Kerem Arıkan, **Abraham Farrell**, Williams Zhang Cen, Jack McMahon, Barry Williams, Yu David Liu, Nael Abu-Ghazaleh, and Dmitry Ponomarev. **TEE-SHirT: Scalable Leakage-Free Cache Hierarchies for TEEs**. In *Network and Distributed Systems Security Symposium (NDSS)*, 2024.

Skills & Interests

Interests: CPU microarchitecture, manycore architectures, scalable memory systems
Languages: C, C++, Python, Verilog
Software: perf, VTune, zsim, SST, Vivado, git, LaTeX, VSCode, CocoTB, MATLAB
Courses: Computer System Organization, Parallel Computer Architectures, Compiler Construction, Parallel Computing, Architectures for Mobile & Edge Computing, Advanced Operating Systems